What Is Claimed Is:

1. A method for fabricating a semiconductor device having a dual damascene interconnecting line structure, comprising the steps of:

providing a substrate having a dielectric layer thereon;

forming a first photoresist layer having a via contact hole pattern on the dielectric layer;

forming a sacrificial layer on the first photoresist layer and filling up the via contact hole pattern;

forming a second photoresist layer having an interconnect trench pattern on the sacrificial layer, thereby exposing the sacrificial layer beneath the interconnect trench pattern;

transferring the interconnect trench pattern to the sacrificial layer using the second photoresist layer as a mask; and

etching the first photoresist layer and the dielectric layer using the second photoresist layer as a mask, thereby transferring the interconnect trench pattern to the dielectric layer and forming an interconnect trench, and continuously etching the dielectric layer along the via contact hole pattern to form a via contact hole in the dielectric layer.

2. The method as claimed in claim 1, wherein the dielectric layer includes a material selected from the group consisting of SiO_2, borosilicate glass (BSG), borophosphate silicate glass (BPSG), fluorosilicate glass (FSG), and tetra-ethyl-ortho-silicate (TEOS).

3. The method as claimed in claim 1, wherein the first and second photoresists are chemically amplified silicon photoresist.

4. The method as claimed in claim 1, wherein the first and second photoresists are selected from different photoresists.

5. The method as claimed in claim 1, wherein the sacrificial layer is I-line photoresist.

6. The method as claimed in claim 1, wherein the depth of the interconnect trench is adjustable by altering etching parameters, thereby changing the etching rate ratio of the first or second photoresist and the etching rate of the sacrificial layer.

7. The method as claimed in claim 1, wherein during etching the sacrificial layer and the first photo resist, the etching rates of the dielectric layer and the first photoresist layer are equivalent.

8. A method for fabricating a semiconductor device having a dual damascene interconnecting line structure, comprising the steps of:

providing a substrate having a metal layer thereon;

forming a dielectric layer on the metal layer;

forming a first photoresist layer having a via contact hole pattern on the dielectric layer;

forming a second photoresist layer on the first photoresist layer and filling up the via contact hole pattern;

forming a third photoresist layer having an interconnect trench pattern on the second photoresist layer, thereby exposing the second photoresist layer under the interconnect trench pattern;

etching the second photoresist layer and transferring the interconnect trench pattern into the second photoresist layer using the third photoresist layer as a mask;

etching the first photoresist layer and the dielectric layer sequentially using the third photoresist layer as a mask, thereby transferring the interconnect trench pattern into the dielectric layer and forming an interconnect trench, and continuously etching the dielectric layer along the via contact hole pattern to form a via contact hole in the dielectric layer;

forming a conductive layer on the dielectric layer and filling the via contact hole and the interconnect trench; and

polishing the conductive layer until the dielectric layer is exposed to achieve a damascene interconnecting line structure with a via contact.

9. The method as claimed in claim 8, wherein the dielectric layer includes a material selected from the group consisting of SiO_2, borosilicate glass (BSG), borophosphate silicate glass (BPSG), fluorosilicate glass(FSG), and tetra-ethyl-ortho-silicate (TEOS).

10. The method as claimed in claim 8, wherein the first and the third photoresists are chemically amplified silicon photoresist.

11. The method as claimed in claim 8, wherein the first and the third photoresists are selected from different photoresists.

12. The method as claimed in claim 8, wherein the second photoresist is I-line photoresist.

13. The method as claimed in claim 8, wherein the depth of the interconnect trench is adjusted by altering etching parameters, thereby changing the ratio of etching rates of the first or third photoresist and the second photoresist.

14. The method as claimed in claim 8, wherein the etching rate of the second photoresist is higher than the etching rate of the first/third photoresist, wherein the ratio of the etching rates is about 5-15:1.

15. The method as claimed in claim 8, wherein during etching the second photoresist and the first photoresist, the etching rate of the dielectric layer and the etching rate of the first photoresist are equal.

16. The method as claimed in claim 8, wherein the conductive layer is metal.

17. The method as claimed in claim 8, wherein the conductive layer is Au, Cu, Ag, Al, W, or alloys thereof.

18. The method as claimed in claim 9, wherein the polishing step comprises chemical mechanical polishing (CMP).